A Combinational Digital Logic Design Tool for Practice and Assessment in Engineering Education

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Abstract

As technology advances, computers are being used almost everywhere. In a 2013 US Census report (File and Ryan, 2014), 83.8% (up from 78.9% in 2012) of U.S. households reported owning a computer with 74.4% reporting internet use (73.4% high speed internet). In recent years, the shift in educational technologies has been moving towards gaming, more specifically serious gaming. Although this is an important trend, there is still much to be said about e-learning through a step-by-step interactive process using an online practice tool. This paper presents a detailed description of the Combinational Logic Design Tool (CLDT) (Morsi and Russell (2007). CLDT was designed and developed under the CCLI project, #0737242, funded by the National Science Foundation, which aimed to develop and disseminate a novel online practice tool for on demand review and assessment in Electrical and Computer Engineering education. The paper also reports on a formal assessment conducted in a Digital Logic Design Classroom and presents the results of this assessment.

Keywords: *digital logic design, assessment, practice, electrical and computer engineering, e-Learning*

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Introduction

In 2013, "83.8% of U.S. households reported owning a computer, with 78.5% of households having a desktop or laptop computer and 63.6% having a handheld computer" (File and Ryan, 2014). It is clear that computers have become a very integral component of our lives and the need continues to use them in the education of the future generation in general and engineering graduates in specific.

Different forms of technology-based education exist but to the best of the author's knowledge, no application exists that is considered to be an online *practice* tool in Digital Logic Design for students in electrical and computer engineering. There are a few online assessment tools in digital logic design that are available to aid in the learning process of students, however their methods give students the option to use them as homework helpers rather than as tools to practice and advance their knowledge of these subjects. The students can, in theory, input a question assigned to them and are given the answer either in a tutorial-like manner or as a correction to a wrong answer being input. This takes away the students' experience of solving the problems themselves which can result in them not knowing whether they have applied the newly learned techniques correctly.

Assessment tools provide the capability of measuring learning. They can also assess the results of a learning activity and its success in enhancing performance. The purpose of this work is to provide a needed addition to existing educational/practice tools for Digital Logic Design, a core course in Electrical, Electronics, and Computer Engineering and Technology programs. The Combinational Logic Design Tool (CLDT) addresses the Combinational Logic Design portion of these curricula. It aids electrical and computer engineering students in the course of their education by providing them with tutorials and randomly generated problem statements to practice on. CLDT randomly generates combinational logic design problems and provides a Just-in-Time assessment of student responses (both textual and graphical).

Some tools currently exist for Digital Logic Design (Digital Simulator (2016), Digital Works (2016), EasySim Digital Logic Simulator (2015), KLogic (2011)) which are considered circuit simulation tools. Other tools exist (Logic circuit simplification, Karnaugh Map Explorer (2011), Karnaugh Map Minimizer (2005)). However, these tools provide solutions to K-Map problems and can be used by students to solve homeworks or assignments they are given in class rather than help them practice what they learned. The goal for Combinational Logic Design Tool (CLDT) was to provide a complete design environment for Combinational circuits. CLDT generates random problem statements for the students to solve and provides a Just-in-Time assessment of student response in a step-by-step fashion (novice) or in a one step process (expert). CLDT cannot be used as a homework helper as it does not provide answers to the problems. It allows the student to learn where s/he went wrong and proceed to correct her/his responses by the use of the assessment results. This way the students can truly practice what they learned, mimicking sitting in a classroom practicing problems with an instructor and learning where they went wrong as they go through solving the problem.

Combinational Logic Design Tool (CLDT)

CLDT was designed to provide random problems for the student to practice combinational logic design by stepping through three sub-tools that include Truth Tables, Karnaugh Maps (K-Maps), and Circuit Design. The tool hosts 3 modules: a truth table generator that randomly generates truth-tables for the student to simplify, a K-Map minimizer that allows students to group the 1's or 0's on a K-Map and create a minimized expression, and a Circuit Design Module which allows the student to build the circuit that represents the minimized expression from the K-Map module (Figure 1). Each module can be used separately or can be used as part of the complete design experience from Truth table to circuit design. At each stage the student can opt to either practice that one module (either Truth Table, K-Map, or Circuit Design) or start at Truth Table or K-Map module and continue with his/her design experience with the remaining modules.

The truth table generator module is able to seamlessly represent its table as a K-Map through the K-Map module, which is the next component of the CLDT. The K-Map module is responsible for generating random expressions for the student to minimize using the K-Map evaluator. The K-Map evaluation should also, instead of only generating expressions, use the expression already generated from the truth-table component. The last component of the CLDT is the Circuit Design Evaluator. This component is to use the minimized expression from the K-Map component to design the circuit that represents the expression. It also generates random expression for students to practice designing using the AND, OR, and NOT gates. The aim of this work is to design a complete combinational logic design tool with Just in Time (JIT) Assessment of user responses for randomly generated problem statements.
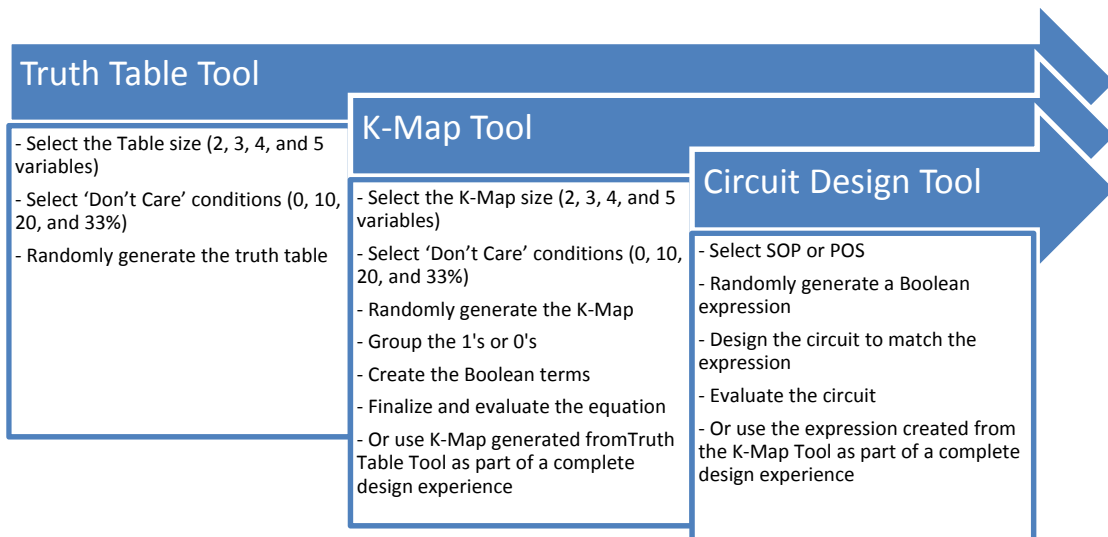
Figure 1. CLDT Tool Structure and Capability

Truth Table Sub-tool

The primary function of this module is to randomly generate truth-tables based on criteria similar to those seen in the K-Map Evaluator tool. This tool allows the student to enter the number of inputs that they want in the expression as well as the percentage of don't care conditions. This will allow them to eventually deduce an expression from the truth table. The truth table module will allow seamless integration of the expressions, realized by the user, into the existing K-Map evaluator tool. This sub-tool is to allow the students to strengthen their knowledge of truth table correlation into Karnaugh maps.

The truth-table module's main functionality is to randomly generate truth-tables based on certain key inputs from the user. These key inputs are, number of input variables and the percentage of "don't care" conditions. Size of the truth-table is within the range of two (2) and five (5) inclusively and you can select between 0, 10, 20 and 33 percent for the "don't care" percentage value.

The truth-table module is the default module of this tool hence it's the first module that is displayed when you start the tool up. However if you are in one of the other tools and would wish to use the truth-table tool again, it's just a matter of selecting the truth-table tab on the tool. An addition based on assessment of the tool in the classroom was to include a score card that shows number of attempts and correctness of those attempts (Figure 2).
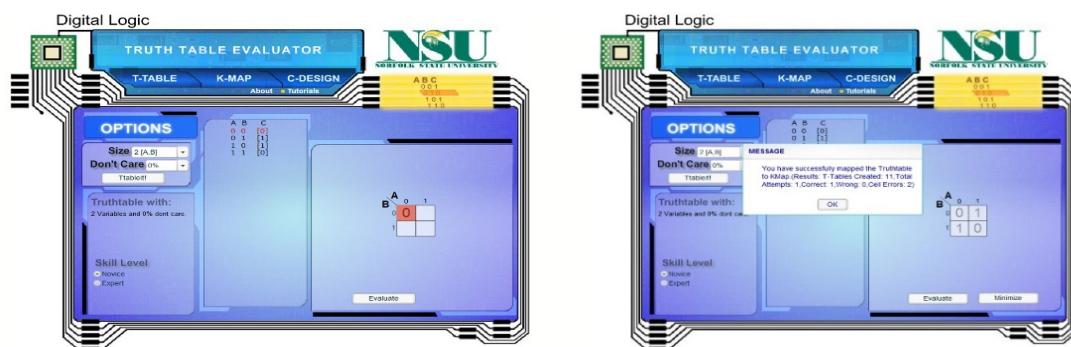

Figure 2. Truth Table sub-tool

K-Map Sub-tool

The K-Map tool provides the user with the ability to randomly generate a K-Map to practice minimization techniques on as well as accepts input from the truth-table module and allows the user to

continue with a complete combinational design experience. It also sends the results to the next stage (the Circuit Design sub-tool) for the user to complete the design of his/her circuit.

The main objective of this sub-tool is to help the students with their skills in minimizing a truth table using K-Maps and producing a minimal Boolean expression. This sub-tool (Figure 3) expects the user to select the size of the K-Map, percent of Don't Cares needed, and whether the user wants to practice grouping for Sum of Products or Product of Sums. Once the map is generated, the user is expected the highlight the groups and enter term by term into the Term Equation box for evaluation (novice), or enter the expression as a whole in the Final equation box (Expert). Once the Final Equation is evaluated and is correct, a button appears for the user to move onto the circuit design portion of the design experience.
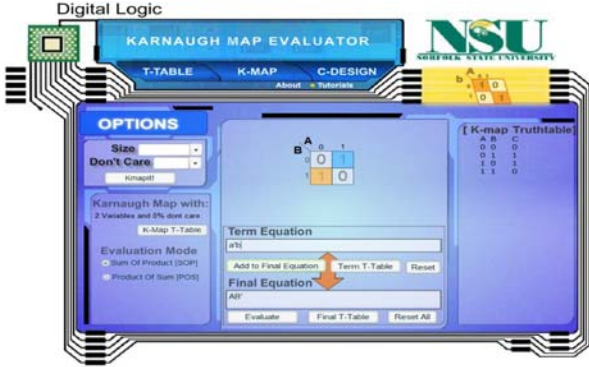

Figure 3. K-Map sub-tool

Circuit Design Sub-tool

This sub-tool is intended to provide practice for students in the design process of combinational circuits using simple gates such as the AND, OR and NOT gates. It allows students to build circuits from expressions completed in the K-Map sub-tool as well as randomly generate algebraic expression for user to practice building circuits on (Figure 4). The core portion of this sub-tool is the Just-In-Time (JIT) assessment of user's graphical responses. The tool checks the final circuit design for correctness and conformity to the algebraic expression under test. It provides instant feedback in a step by step fashion to allow the user the ability to learn from his/her mistakes or to verify his/her knowledge base.
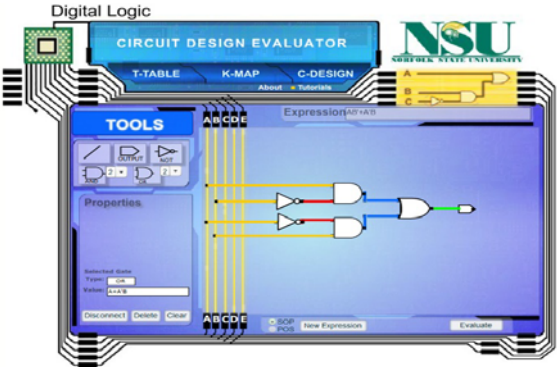

Figure 4. Circuit Design sub-tool

Assessment

CLDT was assessed over two (2) years in the classroom to provide insight into the students' use of the online practice Combinational Logic Design Tool (CLDT) developed to allow students unlimited opportunities to practice circuit design. The students committed to using the tool for

approximately three (3) weeks and afterwards completed post assessments to provide an evaluation of their experience with the tool. To measure the effectiveness of the practice tool, the following questions were used to guide assessment activities. These included:

1. Students will improve in self-monitoring and self-assessment of effective learning strategies.
2. Students will develop a proficiency in using the CLDT practice tools that result in academic achievement in their logic design course.

The main purpose of this project was to develop an on-line practice tool for students enrolled in Digital Logic Design courses. The tool provides a venue for students to practice what they have learned in the classroom, enhance their self-monitoring of learning, as well as allow faculty to use it in a tutorial-like manner.

During two consecutive spring semesters, a total of eighteen (18) students enrolled in the Digital Logic Design course (EEN 231) at Norfolk State University and completed a set of pre-assessments and post-assessments to measure their perceptions of the effectiveness of the CLDT online practice tool for digital logic circuit design after having access to the tool for three (3) weeks. Prior to completing any assessments, the students completed a consent and confidentiality agreement that clearly spelled out their participation in the work, the assessments they would have to complete, and how the data obtained from the assessments would be used. Pre-assessments included measuring learning styles, self-efficacy with learning via technology and levels of difficulty in understanding certain course concepts, frequency of technology use, and demographical data. In addition, students completed a pre-tool-use homework assignment. Finally the students engaged in post-assessments which included a post-tool use-homework assignment on the same concepts covered in the pre-assessment, analysis of journal entries when using the CLDT tool, other assignment grades on the section of the course that included the Truth Tables, K-Maps, and Circuit Design, one Quiz, a Final Exam as the quantitative data, and a focus group.

Pre-Assessments

The pre-assessments for both spring semesters included the gathering of baseline data on the students' preferred learning styles, self-efficacy with learning new problems via technology, and frequency of use with regard to technology. The purpose of these assessments was to control for learning styles, confidence in learning new concepts via technology and controlling for how often, as well as the reasons, students used technology.

Self-Efficacy

The self-efficacy on academic achievement portion of the survey was designed based on Choi, Fuqua, and Griffin's Multidimensional Scales of Perceived Self-Efficacy Survey (2001). Self-Efficacy is a concept that measures an individual's perception of confidence in their ability to do new things in combination with ability to cope with the unknown. Taken together self-efficacy provides a baseline of information regarding the students' perceptions of how well they believe they can learn, retain, and engage in conversations about work that is new and difficult. As a result, the self-efficacy in academic achievement section included questions that asked the students about their perceptions of how well they can learn new concepts, remember information, identify places to study without distractions, motivate themselves to study difficult work, and participate in class discussions when they are unsure about the topic. Two of the questions on learning were in the context of technology based applications. The scale presented on the survey ranged from 1 to 7 representing "not well at all with help" (referred to as low efficacy) to "very well on my own" (referred to as high efficacy).

Learning Styles

The learning styles survey administered to the students was the Index Learning Styles Inventory (ILS) established Felder-Solomon in 1987 specifically for students enrolled in the STEM disciplines, particularly engineering.

Frequency of Technology Use: This section listed seven activities for which the desktop and/or laptop are used and asked the students to indicate the level of frequency they participate in such activities. These included email, instant messaging, Facebook, shopping, researching databases for class work, sending and receiving photos, and uploading or viewing YouTube. The scale used to measure the levels of frequency included (a) Frequently (daily) = 5; Often (2 to 3 times/week) = 4; Sometimes (once a week) = 3; Seldom (2 to 3 times/month) = 2; and Never = 1.

Post-Assessments

The post assessments for both spring semesters included a post-tool-use class assignment to measure whether or not students had improved in their knowledge and understanding of specific

concepts needed for success in the circuit design courses. In addition to pre-post tool use class assessments/assignments, the students also participated in a focus group session to discuss whether or not the practice tool was helpful to their understanding of circuit design as well as offer suggestions on how the tool could be improved.

Student Profile

A profile of the participants from the self-efficacy survey demographics reveals that of the eighteen (18) students who used the CLDT online practice tools, sixteen (16) were male; two (2) were female; seventeen (17) were African American and one (1) identified as other; and seven (7) were sophomores, five (5) were juniors, five (5) were seniors, and one (1) did not indicate class standing. In terms of majors, three (3) were computer science majors and fifteen (15) were electronic engineering majors.

With regard to the learning style profiles, only fifteen of the eighteen students provided their learning styles results. With regard to learning style profiles, the majority were active learners (68%) on Dimension 1 (Active vs. Reflective); majority were visual learners (93%) on Dimension 2 (Verbal vs. Visual); 83% were sensing learners on Dimension 3 (Sensing vs. Intuitive); and 72% were sequential learners on Dimension 4 (Sequential vs. Global). Therefore, the learning style profile revealed that the majority of the students were active, visual, sensing, sequential learners.

Self-Efficacy in Academic Achievement Baseline

The scale presented on the survey ranged from 1 to 7 representing "not well at all" (referred to as low efficacy) to "very well on my own" (referred to as high efficacy). To better understand student responses, the scale was collapsed into five areas (*Not Well at all, Okay with Help, Okay on My Own, Pretty Well with Help, Pretty Well on My Own*). With regard to the survey items on learning, 71% of the students indicated that they could learn new concepts on their own pretty well with help. Specific to learning electrical/digital concepts using technology, 70% could learn pretty well with help, 71% could learn to use electrical/digital circuits pretty well with help, and 59% could design electrical/digital circuits pretty well with help. What this suggests is that students appear to have higher efficacy regarding learning new concepts with technology, learning electrical/digital circuits using technology-based applications, and designing electrical/digital circuits pretty well with help. Given that ten of the seventeen students who completed the evaluations were either in their junior or senior year of the electronic engineering or computer science program, this should be expected.

Table 1. Self-Efficacy in Academic Achievement. Each survey question began with "How well **can** you . . ."

Survey Item (N = 17)	Not Well *at all*	Okay *with help*	Okay *on my own*	Pretty well *with help*	Pretty well *on my own*
1. Learn new concepts using technology based applications or software?	0%	12%	0%	71%	17%
2. Learn math concepts using technology based applications?	0%	12%	6%	70%	12%
3. Learn to use digital circuits?	0%	0%	12%	71%	17%
4. Learn to design digital circuits?	0%	0%	18%	59%	23%
5. Remember new information presented in class?	0%	6%	18%	29%	47%
6. Remember new information presented in the textbooks?	0%	12%	12%	59%	17%
7. Remember new information from hands-on experience?	0%	0%	0%	53%	47%
8. Arrange a place to study without distractions?	6%	6%	12%	17%	59%
9. Motivate yourself to do work that is difficult for you to understand?	0%	6%	18%	29%	47%
10. Participate in class discussions when you are unsure about the topic?	0%	6%	23%	47%	24%

With regard to remembering new information, students responded to survey items that asked how well they could remember new information presented in class, textbooks, or via hands-on practice. Using the same efficacy scale, the majority (76%) could remember what was presented in class pretty well with help or Pretty well on their own. Of the seventeen students, 76% indicated they can remember

new materials from textbooks, 100% could remember new information from hands on experience pretty well with help or pretty well on their own. Again, given the age/maturity and experience of the students in the program, it is expected that more students would indicate a higher efficacy with learning new information and retaining it pretty well on their own.

Finally, when asked about motivation to do difficult work, the majority of the students indicated higher efficacy with 47% indicating they could motivate themselves *pretty well on their own*. Interestingly, only 47% of the students indicated that they could participate in class discussions when they are unsure about the topic *pretty well with help*. The 23% of the students indicated that they could do this okay alone, and 24% indicated they could pretty well alone. See Table 1 for a summary of findings for seventeen of the eighteen students.

Frequency of Technology Use Baseline

The frequency of use of technology section listed seven activities for which the desktop and/or laptop are used and asked the students to indicate the level of frequency they participate in such activities. These included email, instant messaging, Facebook, shopping, researching databases for class work, sending and receiving photos, and uploading or viewing YouTube videos. The scale used to measure the levels of frequency included (a) Frequently (daily) = 5; Often (2 to 3 times/week) = 4; Sometimes (once a week) = 3; Seldom (2 to 3 times/month) = 2; and Never = 1.

As indicated in the research regarding today's youth and their use of desktops and laptops, sixteen of the seventeen students indicated that they email every day and all except fifteen students use their cell phones for reasons other than to make calls, daily. Nine of the students use instant messaging and ten use Facebook daily.

As a result, baseline data indicate that the majority of the students were active, visual, sensing, sequential learners who use computers and various other technologies frequently for various purposes including learning. Their efficacy is higher for learning with technology, various software applications, and even new electrical/digital concepts (learning and designing), but not as high when it comes to participating in discussions when unsure about the topic. As well, the students' efficacy with remembering information when allowed to engage in hands-on practice was rated high as well as their efficacy with motivating themselves to do work that is difficult to understand.

These baseline indicators suggest that the CLDT tool, designed to help students better understand circuit design concepts, should prove beneficial to a group of students who are visual learners, remember better with hands on practice, learn fairly well with technology, and can continue using the tool even when it gets difficult.

Assessment Findings

The post assessments consisted of students logging the amount of time spent using the CLDT practice tool as well as engaging in a one-hour focus group to discuss their perspectives on the tool and providing ways in which the tool could be improved. The findings from each of these assessments are provided below. In the first semester (Group 1) of evaluation, the number of hours worked and whether or not the tool was helpful was asked of the students during the focus group session. However, with the second semester students (Group 2), the number of hours worked was entered onto a journal log and submitted to the evaluator. Therefore, the extent of the information provided on Group 2 students is much greater than that provided on the Group 1 students who shared this information in a focus group.

Group 1 students spent an average of 1 to 1.5 hours working with the CLDT tool. When students were asked to rate how easy it was to use the tool on a scale of 1 to 5 (1 being easy and 5 being difficult), three (3) students rated the ease of use at level 2 while two (2) students rated the ease of use at level 3. For the Group 2 students the seven (7) students spent an average of 3.75 hours on the tool (minimum number of hours was 1.5 and maximum number of hours was 5.5). Of the seven (7) students who reported logged hours with the tool, three (3) worked both novice and expert problems with Truth Tables and four (4) worked with just the expert problems for TT. With regard to the K-Maps, four (4) students worked with both novice and expert problems, while three (3) worked with expert only problems. All students worked on circuit design. Also, of the seven students who logged their work with the CLDT practice tool, four (4) indicated that the tool was "very helpful," two indicated that sometimes the tool was "very helpful" and at other times it was "okay," and only one student indicated that the tool was "okay" only. Finally, of the 231 CLDT problems the students worked as a group, 183 were completed correctly on the first attempt representing a 79% accuracy rate on the first try.

Focus Group after Using CLDT

Both groups of students participated in a focus group after working with the CLDT practice tool. Overall, the students responded to eight (8) questions that asked about the helpfulness of the tool, difficulty of the tool (or user-friendlessness), learning opportunities using the tools, and recommendations for improving the tool. For the Group 1 cohort, seven out of eight students participated in the focus group, and for second semester cohort seven out of ten students participated in the focus group.

Both groups of students indicated that the CLDT practice tool was helpful with Truth-Tables, Karnaugh Maps, and Circuit Design. The students indicated that the tool helps with practicing for tests and quizzes as well as provided everything needed to understand the three concepts mentioned above was included in the CLDT. In addition, Group 2 students specifically indicated that the tools helped them to eliminate steps and allowed for solving more problems. This may explain why, collectively, the students attempted 231 problems getting 183 correct on the first attempt. Finally, the students wanted to have similar opportunities for more difficult design problems.

With regard to difficulty, the students rated the level of difficulty with using the CLDT practice tool as a 2 on a scale of 1 to 5—with 1 representing easy and 5 representing difficult. When the students were asked why they rated the level of difficulty as a 2, most of the responses were related to the alignment of the square in the Truth-Tables and the size of the space for circuit design. In addition, the students indicated that the connectivity for the circuit should be rechecked since there were times when they could not pull up the gate because "the circuit part tells you it's not connected." It is important to note here that these issues have been corrected in the final version of the tool.

Conclusions

Assessment Summary

The CLDT practice tool has proven to be very helpful to students with regard to practicing Truth Tables, Karnaugh Maps, and Circuit Design in the Digital Logic Design Course in the Engineering Department at Norfolk State University. Baseline data support the likelihood that students would be more likely to improve their learning by using online tools particularly with emphasis on high self-efficacy for learning with technology and learning new materials presented in class with hands-on practice. All the participating students are active, visual, sensing, and sequential learners which suggest that students learn best when they can "try things out," learn from "sights, sounds, and physical sensations," "see pictures and graphs," and "learn how to solve problems in a step-by-step manner."

With regard to the difficulty with using the CLDT practice tool, all students gave the tool a rating of 2 while a few indicated 3—both of which means that the students believed the CLDT tool to be easy to navigate. With this rating the students provided reasons why they did not choose #1 as the response for "very easy." Reasons for rating the tool at a level of 2 instead of 1 referred to the "lack of alignment of connectivity to pull the gate up," "not knowing where you went wrong if you get an answer incorrect," and "trying to figure out how to work a problem that is correct". Also, students would definitely recommend the CLDT practice tool to other students at NSU as well as other institutions if the above concerns were addressed. In addition, students would like to see a larger space to design circuits.

Academic Achievement

In addition to the above assessments, the Group 1 students completed two homework assignments (one before the practice tool--HW4, and one after the practice tool--HW5) and the second semester students completed two pre-tool homework assignments (HW4 and HW5) and completed one set of homework problems after working with the CLDT practice tool (HW6).

With regard to academic achievement, both groups of students realized a higher grade from pre-tool-use to post-tool-use. As the students indicated, the practice tool helped them to improve in their work. For group 1, overall, students received an average score of 47.1% on the circuit design concepts before using the tool and an average score of 72.6% after using the tool representing a 25.5% increase in performance. For group 2, the increase was somewhat smaller (but still a significant increase) in that the average score before using the tool was 57% and 76% after using the tool representing a 19 point increase in performance.

Ultimately, the CLDT tool helped the students perform better in their course work, including quizzes and tests, with Equation to Circuit Design and K-Map to Equation creation. In addition, the students' number of correct responses on homework problems increased for almost all aspects.

Final Remarks

The CLDT Tool was designed and developed through support from a National Science Foundation grant. The tool was assessed over a two year period in a Digital Logic Design class which is offered once a year in the spring semester. Overall, the CLDT practice tool has proven to help students improve in their learning as well as in monitoring their learning. Students also had the opportunity in participating in improving the tool through their assessment.

Some issues were encountered by the students who piloted the tool. These included:

- "Add a time limit on "expert" level for circuit design
- Fix broken info link
- Give hints on what's wrong or the theorem to refer
- Directions needed
- Track number of problems to show how you improved--a scoreboard
- Set up like a practice test where you are timed and scored
- Widen the space and provide more area in circuit design—bigger image, space to work with the circuit.
- Improve the circuit design and make it less difficult to connect the gates to one another.
- The actual program is in a small space on the screen—enlarge it."

Most issues encountered by the students (truth table cell highlights, drawing area for circuit needing increase, include directions, broken links, timed testing, scoreboard, etc.) and mentioned in the assessments have been corrected. Some issues were not addressed such as not being provided a solution since the main concept behind CLDT was to provide a practice tool and not a homework helper.

In conclusion, the purpose of this work was to provide a needed addition to existing educational/practice tools for Digital Logic Design. CLDT aids electrical and computer engineering students in the course of their education by providing them with randomly generated problem statements to practice on. CLDT randomly generates combinational logic design problems and provides a Just-in-Time assessment of student responses (both textual and graphical). It has proven to be a valuable tool in improving student achievement in the classroom.

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